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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/909,562	07/20/2001	Yakov Tokar	SC0361WI	2577

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MOTOROLA INC
AUSTIN INTELLECTUAL PROPERTY
LAW SECTION
7700 WEST PARMER LANE MD: TX32/PL02
AUSTIN, TX 78729

EXAMINER	
MOAZZAMI, NASSER G	
ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 10/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/909,562	Applicant(s) Tokar et al.
	Examiner Nasser Moazzami	Art Unit 2187

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *Three* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jul 20, 2001* .

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-14* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☒ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on *Jul 20, 2001* is/are a) ☒ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). *2*
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. The formal drawings submitted on 07/20/2001 have been approved by the office draftsman.

Specification

2. Claims 1-14 are presented for examination.

3. The disclosure is objected to because of the following informalities: the text for the heading "brief summary of the invention" (page 4) is not included in the specification as required by Patent Rule 1.73.

A brief summary of the invention indicating its nature and substance, which may include a statement of the object of the invention, should precede the detailed description. Such summary should, when set forth, be commensurate with the invention as claimed and any object recited should be that of the invention as claimed. (See MPEP 608.01(d)). Applicant is required to restrict the brief summary of the invention to descriptive matter so as to be in harmony with the claims (MPEP 1302.01).

Appropriate correction is required.

4. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

5. Applicant is reminded of the duty to fully disclose information under 37 CFR 1.56.

6. The Information Disclosure Statement received 07/20/2001 has been considered. Please see attached PTO-1449.

Claim Objections

7. Claims 3-5, and 8-14 are objected to because of the following informalities:

Claim 3

Line 9, --and-- should be added after "provided;".

Claim 8

Line 2, --a-- should be inserted before "plurality".

Claim 10

Line 5, "cached" should be changed to --cache--.

Claim 12

Line 5, "cached" should be changed to --cache--.

Claims 4-5, 9, 11, and 13-14 are objected as being dependent upon an objected claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Ng (U.S. Patent No. 5,623,608).

Ng teaches a system and a method for managing a buffer. Ng further discloses an initial request to access a desired data which is going to be presented to the buffer memory (cache) first and if it misses the cache, it will be presented to the slower memory to be retrieved and to be store in the cache and to be sent to the processor. While it is retrieving the requested data, it will prefetch additional data consecutive to the initial data

to be stored in the cache for future use. If another request (second or third) request is initiated while the data is being prefetched, based on whether the another request is part of addresses that is being prefetched or not, the prefetching either is going to be interrupted or continue.

As for claim 1, Ng teaches a method for filling a line in a cache, comprising the steps of: sending a request for data to be provided on a data bus to the cache at a first address ***[the purpose of the cache in every computer system is to increase access speed to the data, so initial read request from the processor first goes to the cache (column 1, lines 21-25, and lines 36-37; column 5, lines 58-60; column 8, lines 29-30; and see step 64 of figure 3B)]***; sending a first request external to the cache for first data at the first address ***[if there is a cache miss, the request will be provided to the slower memory such as slow RAM, DASD or Optical disk (see figure 1; and step 90 of figure 3B)]***; sending for additional data at additional addresses, the additional addresses being consecutive with the first address ***[after completion of the fetch operation, the data store continues to read in consecutive order sufficient***

additional subsequent data blocks to fill the active buffer memory segment (column 1, lines 51-54)]; receiving the first data located at the first address and placing the first data in the line in the cache and onto the data bus ; loading the additional data into the line in the cache as it is received ***[the data store first fetches the requested data blocks and stores it in the buffer memory; the external processor receives data blocks on the bus in response to the same data access request; a requested data block is stored and subsequent prefetched data blocks are written in consecutive order to the segment in the buffer memory (column 1, lines 49-51; column 5, lines 58-61; and column 6, lines 7-11)];*** terminating the loading of the additional data in response to a second request for different data that is at a different address from the additional addresses; and sending the second request external to the cache for the different data at the different address ***[if the data access request is not in the buffer memory and is not in the prefetching range, immediately halting the present prefetching access to initiate the new fetching access (column 8, lines 28-43; also see figures 3A and 3B)].***

As for claim 2, Ng teaches continuing loading the additional data into the line in the cache as it is received in response to receiving a data request at one of the additional addresses for data not present in the cache ***[if the data access request finds that the requested data block is not in the buffer memory, but it is in the prefecthing access in progress, waiting for completion of the present prefetching (column 8, lines 28-35; also see figures 3A and 3B)]***.

As for claims 3-5, Ng teaches a method for operating a processing system comprising a cache and a processor ***[buffer memory and processor (see column 1, lines 23-24 and figure 1)]***, claims 3-5 encompass the same scope of the invention as those of the claims 1, and 2. Therefore claims 3-5 are rejected for the same reasons as stated above in regard to claims 1, and 2.

As for claims 6-9, Ng discloses a processing system ***[system 10 (see figure 1)]*** with a number of units for performing the step functions of the method claims 1, and 2, wherein the cache is characterized as having a plurality of lines that each comprise locations having consecutive addresses ***[buffer memory 26***

organized as a plurality of memory segments, each segment provides for contiguous storage of 32 data blocks (column 5, lines 62-67; also see figure 2)]. Therefore claims 6-9 encompass the same scope of the invention as those of the claims 1, and 2 and are rejected for the same reasons as stated above with respect to claims 1, and 2.

As for claims 10-14, Ng discloses a processing system ***[system 10 (see figure 1)]*** with a number of units for performing the step functions of the method claims 1, and 2, wherein the cache is characterized as having a plurality of lines that each comprise locations having consecutive addresses ***[buffer memory 26 organized as a plurality of memory segments, each segment provides for contiguous storage of 32 data blocks (column 5, lines 62-67; also see figure 2)]***, and providing a hit signal if a request for data is contained in the cache and a miss signal if the request for data is not contained in the cache ***[buffer hit and buffer miss (column 1, lines 56-61; and column 8, lines 28-36; also see figure 3B step 64)]*** . Therefore claims 6-9 encompass the same scope of the invention as those of the claims 1, and 2

and are rejected for the same reasons as stated above with respect to claims 1, and 2.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,233,656 (Jones et al.) discloses a system for optimizing bus bandwidth, wherein the bus accesses a range from a single word by prefetching and caching additional words when corresponding to a single word access request.

U.S. Patent No. 6,219,760 (McMinn) teaches a cache memory with a number of ways, wherein at least one way is assigned for prefetching.

U.S. Patent No. 6,138,212 (Chiacchia et al.) discloses a computer system with a single ported data cache and a dual ported prefetch cache, wherein when a data cache miss occurs, the requested data is loaded into the data cache and into prefetch cache. Thereafter, each data request that hits in the prefetch cache will results in prefetching of data into prefetch cache.

U.S. Patent No. 5,649,144 (Gostin et al.) teaches a processing system with a means to generate a memory address and means to present the address to the cache, if there is a cache miss, the requested data is loaded from main memory and prefetching additional addresses into the cache.

11. When responding to the office action, applicant are requested to provide examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any response to this action should be mailed to:

Commission of Patent and Trademarks

Washington, D.C. 20231

12. Any inquiry concerning this communication from the examiner should be directed to Nasser Moazzami whose telephone number is (703) 305-0017 from 8:00am-5:30pm on Monday-Friday or to the examiner's supervisor, Do Yoo who can be reached at (703)308-4908 on Monday-Friday from 8:00am-4:30pm EST.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (703)305-3900.

The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communication.

13. A shortened statutory period for response to this action is set to expire 3 (three) months from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

Nasser Moazzami

Examiner

10/17/2002